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Design of CMOS Inverter using SNWFET on Nanohub

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Abstract

In this paper a layout design of an ultra-compact CMOS inverter using silicon nanowire field effect transistor with minimal power dissipation while matching the transient performance of bulk and SOI CMOS circuits is proposed. In this study, we took into account the strengths of nanotechnology including low static and dynamic power dissipation, suppression of short channel effect (SCE) and drain-to-source breakdown voltage, surface mobility enhancement and the ease of manufacturability. We analyzed different component which gives low static power dissipation. Once the body dimensions are determined, dc characteristics of the optimal n and p-channel transistors are evaluated in terms of SCE, DIBL, drain-to-source breakdown voltage and noise margin (NM). In this paper layout extraction is presented, which is a method of achieving low dynamic power dissipation.

Key words: Inverter, Nanotechnology, Nanowire FET, CMOS, VLSI Design.

1. Introduction

Scaling down the dimension of each transistor is the basic element of integrated circuit, thus increasing the total number of transistors in a chip[1]. Device scaling is essential for getting the ride of successive improvement in IC technology. As the MOSFET gate length enters the nanometer regime, short channel effects (SCE) such as threshold voltage (V_T) roll-off and drain induced barrier lowering (DIBL) become increasingly significant, which limits the scaling capability of planar bulk or silicon-on-insulator (SOI) MOSFET [2]. At the same time relatively low carrier mobility in silicon, compared to other semiconductor, may also degrade the MOSFET device performance, *i.e.* ON current and intrinsic device delay[3]. For these reasons various novel device structures and materials like silicon nanowire transistors, carbon nanotube FETs, new channel materials (e.g. strained silicon, pure germanium) molecular transistor are being extensively exposed by researchers[4,5,6,7,8].

Among all these promising post-CMOS structure, the silicon nanowire transistor (SNWT) has its unique advantage. The SNWT is based on silicon, a material over which semiconductor industry has been working on for more than forty years. It would be really attractive to stay on silicon and also achieve good device metrics that is expected from nanoelectronics.

2. NMOS and PMOS SNWT design

2.1 Design Consideration to Achieve Low Static Power Dissipation in SNWT.

There are three major OFF current components that produce low static power dissipation: junction leakage, sub-threshold leakage, and gate-induced-drain-leakage (GIDL) current. Junction leakage current primarily depends on DIBL factor as expressed as:

$$DIBL = \frac{V_{TSAT} - V_{TLIN}}{V_{DD} - V_{DS}} \tag{1}$$

Where, V_{TLIN} and V_{TSAT} are the threshold voltages at V_{DS} = 50 mV and V_{DD} respectively. Sub threshold leakage current is a function of sub threshold slope and saturation threshold voltage; it is expressed as:

$$I_{SUB} = I_0 - V_{TSAT}/S \tag{2}$$

Where I_0 is the drain current at $V_{GD} = V_{TLIN}$ and S is given as:

$$S = \frac{kT}{q} \log\left(1 + \frac{C_D}{C_{ox}}\right) \tag{3}$$

In this equation C_D and C_{OX} is channel depletion region and gate oxide capacitances respectively. The third component I_{GIDL} current is a strong function of transverse electric field E_S at the semiconductor surface perpendicular to the device axis and is given as:

$$I_{GDIL} = A.E_s \exp\left(\frac{-B}{E_s}\right) \tag{4}$$

Where,

$$E_s = \frac{V_{DG} - V_{FB} - 1.2}{3t_{ox}} \tag{5}$$

A and B is constant, V_{DG} is the drain-to-gate potential, V_{FB} is flat band voltage t_{ox} and is the oxide thickness. Therefore OFF current can be reduced by decreasing DIBL, t_{ox} body doping concentration, and ε_s. In the proposed layout, t_{ox} is set to a minimum value of 1.5 nm to maintain the gate leakage current to a negligible level with respect to I_{OFF}. The body doping concentration is reduced to intrinsic level to minimize C_D and ε_s is also kept small due to non-overlapping gate-drain region.

2.2 Device Structure :

Both NMOS and PMOS transistors are designed as enhancement- type with uniform undoped silicon bodies constructed perpendicular to the substrate. Source/drain (S/D) contacts are assumed to have Gaussian profiles with a peak doping concentration of 10 cm. Both n and p -channel transistors have metal gates of 1.5 nm thick gate oxide.

2.3 Metal Gate Work Function Values for NMOS and PMOS Transistors :

The first task of this design process is to determine an individual metal work function for each minimum

length NMOS and PMOS transistor to produce a threshold voltage of approximately 300 mV. This value constitutes 30% of the 1 V power supply voltage and provides sufficient noise immunity for safe large-signal circuit operation. Therefore, threshold voltage of a 5 nm (minimum) channel length device is first measured as a function of work function for each body radius from 1 to 25 nm as shown in Fig. 1. Longer channel length devices yield marginally higher threshold voltages and improve noise margin safety for large-signal circuit operations. The intersection of threshold voltage with 300 mV level in Fig 1 is projected to the x axis to yield an individual work function for each NMOS and PMOS transistor at a different body radius.

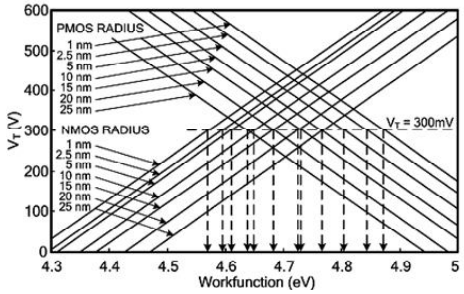

Figure 1: Threshold voltages of NMOS and PMOS nanowire transistors as a function of metal work function at a minimum effective channel length of 5 nm. Radius of both NMOS and PMOS transistors is changed between 1 and 25 nm.

2.4 OFF Current Requirement :

The leakage current is an important factor towards lowering overall standby power consumption; both NMOS and PMOS transistors are designed to have static leakage currents smaller than 1 pA which is significantly smaller than SOI transistors in earlier modeling studies and several orders of magnitude smaller than the current technology trend.

2.5 Intrinsic Transient Time :

Intrinsic transient time determines the time interval for a transistor to charge (or discharge) the gate capacitance of an identical transistor when it is fully on and is a quick way to understand the transient characteristics of an individual transistor without building any circuitry. The intrinsic transient time of each qualified transistor is measured as shown in Fig. 2

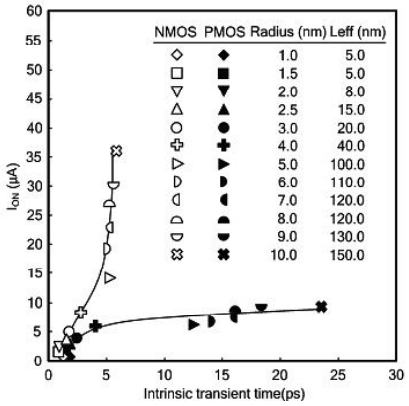

Figure 2: ON current versus intrinsic transient time of the NMOS and PMOS nanowire transistors whose leakage current is below 1 pA.

In this figure, ON currents of the qualified NMOS and PMOS transistors start diverging after device geometry of 4 nm radius and 40 nm effective channel length larger wire radius provides higher I_{ON} values for NMOS transistors, but reaches a saturation plateau for PMOS transistors. Therefore, the 4 nm radius and 40 nm effective channel length device geometry is considered an optimal choice to produce approximately equal drive currents and intrinsic transient times for both NMOS and PMOS transistors.

3 CMOS- SNWT Inverter Layout :

Fig. 3 shows the cross section and the corresponding layout of a single SGFET. The active region defines the circular body of the SGFET, which is surrounded by n^+ well if the transistor is an n-channel device or p well if it is a p -channel. The outmost circle represents the metal gate. All contacts are indicated by 2.4 nm by 2.4 nm black squares touching the drain the source and gate of the transistor.

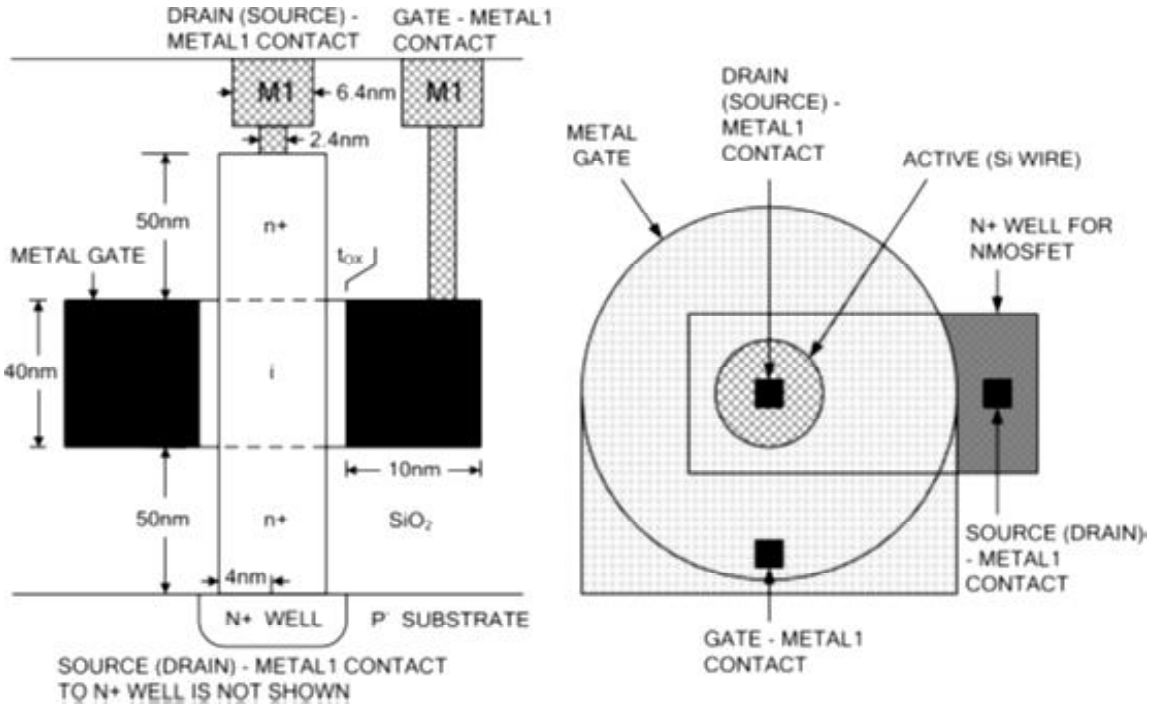

Figure 3: Cross section and layout topology of a single SNWT NMOS transistor.

A CMOS inverter layout designed by nMOS and pMOS silicon nanowire transistors are shown as in which the vertical diamention is fix where each circular node corresponds to vertical nMOS or PMOS interconnections are steblised by 6.4 nm wide metal 1 and metal 2 wire. Inverter input and out terminals are formed by connecting the gate extention and the drain with a metal 1 layer and a single contact ,respectively. Power and ground connections are made to p^+ and n^+ wells with multiple contacts, a metal 1 layer , and a metal 2 layer. p^+ well is completaly surrounded by an n- well to prevent latchup.

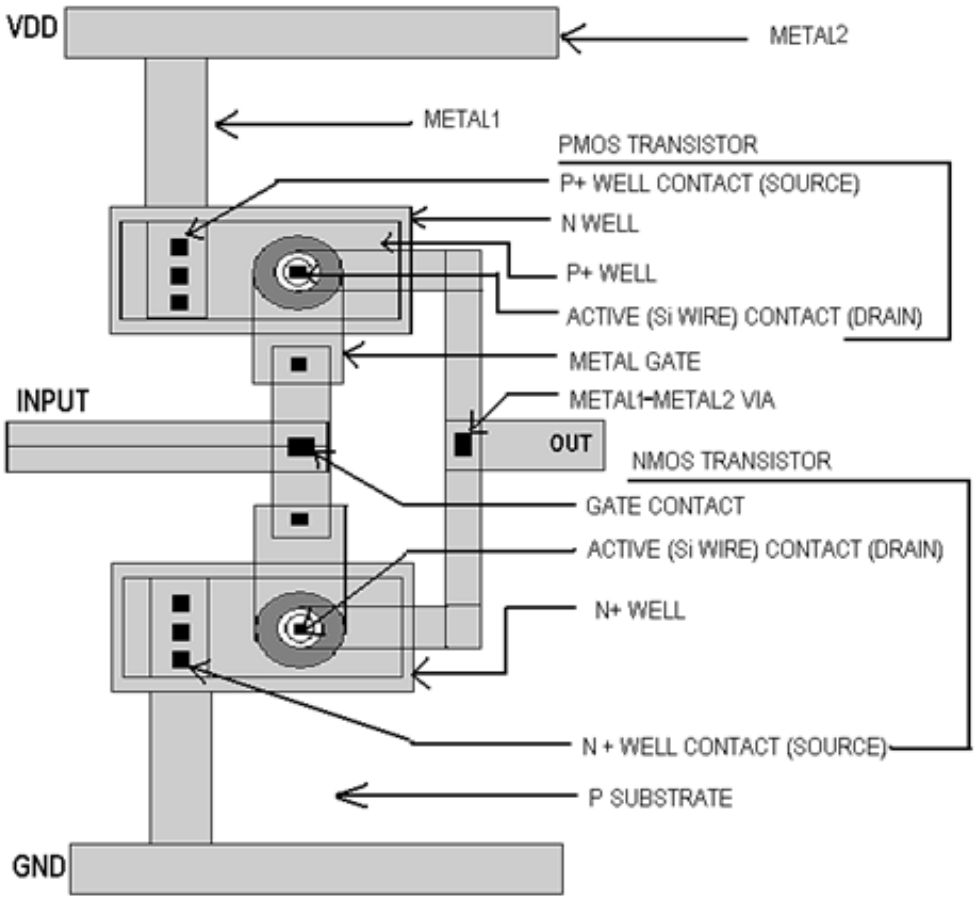

Figure 4.5 CMOS inverter using nMOS and pMOS silicon nanowire transistors.

4. Power Dissipation :

Worst case power dissipation is composed of static power dissipation and dynamic power dissipation which is a function of frequency of operation $f_{OP,}$ power supply voltage and load capacitance as :

$$P_{diss} = f_{op} . C_L . V_{DD}^2 \quad (6)$$

Where V_{DD} and f_{op} when adjusted for optimum circuit performance and at nanometer scale, the only possible variable to control is the load capacitance C_L. Even though the dimensions of a bulk transistor can be changed to have the same gate capacitance of a single nanowire transistor, impact ionization, punch-through effect and high S/D capacitance are still potential problems for the bulk device. Dual-gated SOI transistors benefit the same advantages of nanowire transistors, but their gate capacitance, and therefore the dynamic power dissipation, doubles as shown in above.

5. Conclusion

The design of CMOS inverter using silicon nanowire transistor is presented, which gives the better performance, less power consumption, less area than the planner CMOS inverter. The design is optimized for

low power VLSI architecture, simulated on the online simulation tool provided by www.nanohub.org. On comparing the results reported previously for silicon bulk and double-gated SOI transistors, our findings indicate the silicon nanowire technology may be a potential choice for the future of VLSI circuits because of its low power dissipation in a compact layout area.

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