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Architectures for Realization of Two-Dimensional Discrete Sine Transform

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Abstract

In this paper, two algorithms for realizing two-dimensional discrete sine transform (2-D DST) are proposed. Basing on these two algorithms, two systolic architectures are presented for implementing 2-D DST of even *N*. The systolic array using the algorithm-1 is a bilayer structure, which does not require any hardware/time for the transposition of the intermediate results.

Key words : Discrete sine transform; Discrete cosine transform; Systolic architecture.

1. Introduction

The Discrete sine transform (DST) was first introduced to the signal processing by Jain[1], and several versions of this original DST were later developed by Kekre *et al.*[2], Jain[3] and Wang *et al.*[4]. There exist four even DST's and four odd DST's, indicating whether they are an even or an odd transform[5]. Ever since the introduction of the first version of the DST, the different DST's have found wide applications in several areas in Digital signal processing (DSP), such as image processing[1,6,7], adaptive digital filtering[8] and interpolation[9]. The performance of DST can be compared to that of the discrete cosine transform (DCT) and it may therefore be considered as a viable alternative to the DCT. For images with high correlation, the DCT yields better results; however, for images with a low correlation of coefficients, the DST yields lower bit rates[10]. Yip and Rao[11] have proven that for large sequence length ($N \geq 32$) and low correlation coefficient ($\rho < 0.6$), the DST performs even better than the DCT.

In this paper, two algorithms for 2-D DST are presented. Then these two algorithms are implemented by two systolic architectures. The systolic architecture using algorithm-1 is a bilayer structure, which does not require any hardware/ time for the transposition of intermediate results.

The systolic architecture has the following characteristics:

- A massive and non-centralized parallelism
- Local communications
- Synchronous evaluation

The systolic arrays are used in the design and implementation of high performance digital signal processing equipment. Systolic architectures are established as the most popular and dominant class of VLSI structures due to the simplicity of their processing elements (PEs), modularity of their structure, regular and nearest neighbour interconnections between the PEs, High level of pipelinability, small chip area and lower dissipation. In the systolic architectures, the desired data are pumped rhythmically in regular intervals across the PEs for yielding high throughput by fully pipelined processing. The systolic array concept can also be exploited at bit level in the design of individual VLSI chips. The highly regular structure of systolic circuits renders them comparatively easy to design and test.

The rest of the paper is organized as follows. The proposed algorithm-1 for 2-D DST is presented in Section-2. The systolic architecture for implementation of 2-D DST using algorithm-1 is presented in Section-3. The algorithm-2 for 2-D DST is derived in Section-4. The systolic architecture for realizing 2-D DST using algorithm-2 is presented in Section-5. Conclusion is given in Section-6. Finally references are given in Section-7.

2. Proposed algorithm-1 for 2-D DST :

For a given input data sequence x_{ij}, the 2-D DST for output data sequence Y_{mn} is defined by

$$Y_{mn} = \frac{2}{N} a_m a_n \sum_{i=1}^{N}\sum_{j=1}^{N} x_{ij} \sin\left[\frac{(2i-1)m\pi}{2N}\right] \sin\left[\frac{(2j-1)n\pi}{2N}\right] \qquad (1)$$

for $m, n = 1,2,\ldots,N$
where

$$a_k = \begin{cases} \frac{1}{\sqrt{2}}, & \text{if } k = N \\ 1, & \text{if } k = 1, 2, \ldots, N-1 \end{cases} \qquad (2)$$

Without loss of generality, the scale factor $2 a_m a_n / N$ may be ignored in the rest of the paper. Also N is assumed to be even throughout the paper.
Let

$$S_{rk} = \sin\left[\frac{(2k-1)r\pi}{2N}\right] \qquad (3)$$

Then (1) may be written as

$$Y_{mn} = \sum_{i=1}^{N}\sum_{j=1}^{N} x_{ij} S_{mi} S_{nj}$$

$$= \sum_{j=1}^{N} W_{mj} S_{nj} \qquad (4)$$

where $W_{mj} = \sum_{i=1}^{N} x_{ij} S_{mi}$ (5)

The output data Y_{mn} is realized in two stages. In the first stage, W_{mj} is computed from x_{ij} using (5). In the second stage, Y_{mn} is computed from the intermediate result W_{mj} using (4).

3. Systolic architecture for implementation of 2-D DST using algorithm-1 for N = 4

The 2-D DST given in algorithm-1 is realized by the systolic architecture for $N = 4$ as per the following two steps.

1. W_{mj} is computed using (5)
2. Y_{mn} is computed using (4)

***Step1*:**
Equation (5) for $N = 4$ can be written as

$$W_{mj} = \sum_{i=1}^{4} x_{ij} S_{mi} \qquad (6)$$

for $j = 1,2,3,4$ and $m = 1,2,3,4$.
From (6), we get the following 16 expressions for all values of j and m.

$$W_{11} = x_{11}S_{11} + x_{21}S_{12} + x_{31}S_{13} + x_{41}S_{14}$$
$$W_{12} = x_{12}S_{11} + x_{22}S_{12} + x_{32}S_{13} + x_{42}S_{14}$$
$$W_{13} = x_{13}S_{11} + x_{23}S_{12} + x_{33}S_{13} + x_{43}S_{14}$$
$$W_{14} = x_{14}S_{11} + x_{24}S_{12} + x_{34}S_{13} + x_{44}S_{14}$$
$$W_{21} = x_{11}S_{21} + x_{21}S_{22} + x_{31}S_{23} + x_{41}S_{24}$$
$$W_{22} = x_{12}S_{21} + x_{22}S_{22} + x_{32}S_{23} + x_{42}S_{24}$$
$$W_{23} = x_{13}S_{21} + x_{23}S_{22} + x_{33}S_{23} + x_{43}S_{24}$$
$$W_{24} = x_{14}S_{21} + x_{24}S_{22} + x_{34}S_{23} + x_{44}S_{24} \qquad (7)$$
$$W_{31} = x_{11}S_{31} + x_{21}S_{32} + x_{31}S_{33} + x_{41}S_{34}$$
$$W_{32} = x_{12}S_{31} + x_{22}S_{32} + x_{32}S_{33} + x_{42}S_{34}$$
$$W_{33} = x_{13}S_{31} + x_{23}S_{32} + x_{33}S_{33} + x_{43}S_{34}$$
$$W_{34} = x_{14}S_{31} + x_{24}S_{32} + x_{34}S_{33} + x_{44}S_{34}$$
$$W_{41} = x_{11}S_{41} + x_{21}S_{42} + x_{31}S_{43} + x_{41}S_{44}$$
$$W_{42} = x_{12}S_{41} + x_{22}S_{42} + x_{32}S_{43} + x_{42}S_{44}$$
$$W_{43} = x_{13}S_{41} + x_{23}S_{42} + x_{33}S_{43} + x_{43}S_{44}$$
$$W_{44} = x_{14}S_{41} + x_{24}S_{42} + x_{34}S_{43} + x_{44}S_{44}$$

The first step for realization of 2-D DST algorithm -1 is done by systolic array-1, shown in Fig. 1. It consists of N^2 identical PEs. The 0s in Fig.1 denote the delays. The sine kernels are generated by a kernel generating processor. The function of each PE in systolic array-1 is shown in Fig. 2. Each PE comprises of one adder, one multiplier and one accumulator. Each PE computes W_{ij} in N time-steps. The intermediate values $W_{11}, W_{12}, \ldots\ldots, W_{44}$ given in (7) accumulate in PE1, PE2, ……, PE16 respectively.

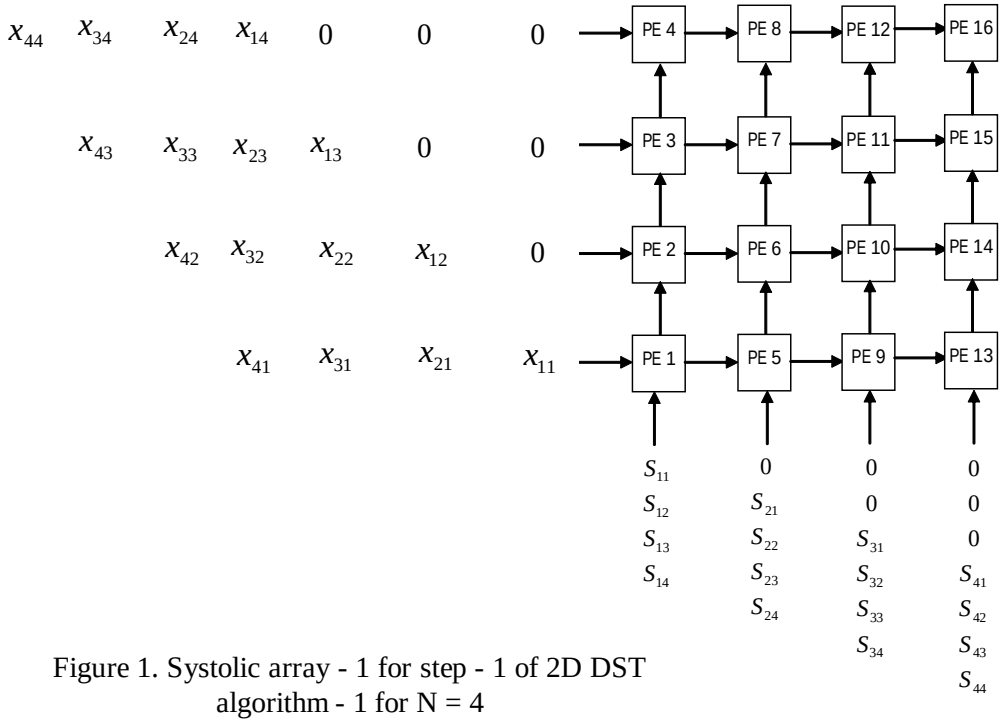


Figure 1. Systolic array - 1 for step - 1 of 2D DST algorithm - 1 for N = 4

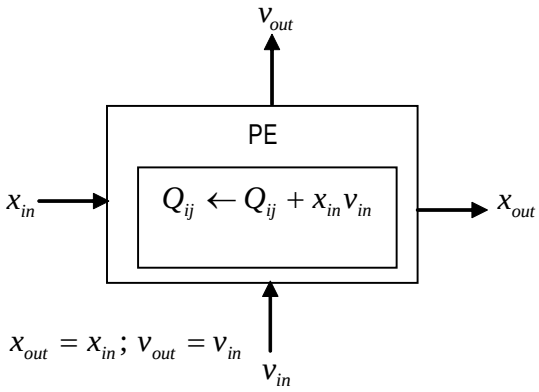


Figure 2. Function of each PE of systolic array – 1

***Step2*:**

Equation (4) for $N = 4$ can be expressed as

$$Y_{mn} = \sum_{j=1}^{4} W_{mj} S_{nj} \qquad (8)$$

for $m = 1,2,3,4$ and $n = 1,2,3,4$.

From (8), we can write the following 16 expressions for all values of m and n.

$Y_{11} = W_{11}S_{11} + W_{12}S_{12} + W_{13}S_{13} + W_{14}S_{14}$

$Y_{12} = W_{11}S_{21} + W_{12}S_{22} + W_{13}S_{23} + W_{14}S_{24}$

$Y_{13} = W_{11}S_{31} + W_{12}S_{32} + W_{13}S_{33} + W_{14}S_{34}$

$Y_{14} = W_{11}S_{41} + W_{12}S_{42} + W_{13}S_{43} + W_{14}S_{44}$

$Y_{21} = W_{21}S_{11} + W_{22}S_{12} + W_{23}S_{13} + W_{24}S_{14}$

$Y_{22} = W_{21}S_{21} + W_{22}S_{22} + W_{23}S_{23} + W_{24}S_{24}$

$Y_{23} = W_{21}S_{31} + W_{22}S_{32} + W_{23}S_{33} + W_{24}S_{34}$

$Y_{24} = W_{21}S_{41} + W_{22}S_{42} + W_{23}S_{43} + W_{24}S_{44}$ (9)

$Y_{31} = W_{31}S_{11} + W_{32}S_{12} + W_{33}S_{13} + W_{34}S_{14}$

$Y_{32} = W_{31}S_{21} + W_{32}S_{22} + W_{33}S_{23} + W_{34}S_{24}$

$Y_{33} = W_{31}S_{31} + W_{32}S_{32} + W_{33}S_{33} + W_{34}S_{34}$

$Y_{34} = W_{31}S_{41} + W_{32}S_{42} + W_{33}S_{43} + W_{34}S_{44}$

$Y_{41} = W_{41}S_{11} + W_{42}S_{12} + W_{43}S_{13} + W_{44}S_{14}$

$Y_{42} = W_{41}S_{21} + W_{42}S_{22} + W_{43}S_{23} + W_{44}S_{24}$

$Y_{43} = W_{41}S_{31} + W_{42}S_{32} + W_{43}S_{33} + W_{44}S_{34}$

$Y_{44} = W_{41}S_{41} + W_{42}S_{42} + W_{43}S_{43} + W_{44}S_{44}$

The output components Y_{mn} are computed from the intermediate results W_{ij} using the systolic array-2, shown in Fig. 3. It consists of N^2 identical PEs and the function of each PE is shown in Fig. 4. Each PE consists of one multiplier, one adder and one register.

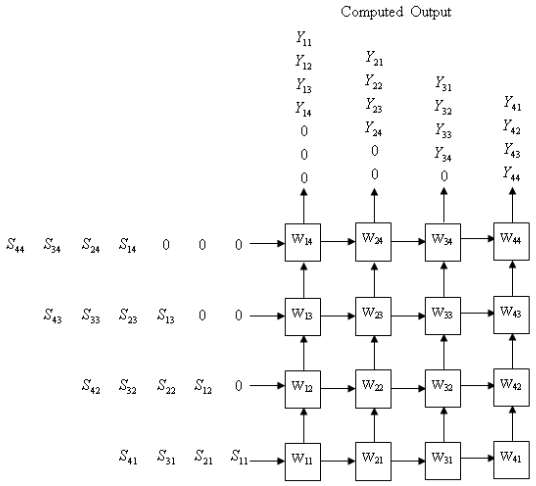


Figure 3. Systolic array – 2 for step – 2 of 2D DST algorithm – 1 for $N = 4$

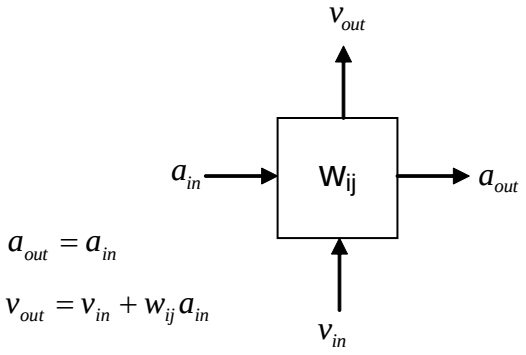


Figure 4. Function of each PE of systolic array – 2

The proposed systolic architecture for implementation 2-D DST algorithm-1 is a bilayer structure consisting of two layers of systolic arrays placed over one another. The systolic array-2 is placed over the systolic array-1, such that each PE in the upper layer is over a PE of the lower layer. The lower layer makes the first stage of computation to provide the intermediate result W_{ij} to the upper layer. Each value of W_{ij} is stored in the register of each PE of the upper layer. The upper layer makes the second stage of computation to yield the desired 2-D DST components Y_{mn}. The systolic array-2 in the upper layer computes each output component Y_{mn} in N time-steps.

As the expressions in (7) and (9) can be expressed by matrices, the systolic array-1 and -2 can used for matrix multiplication.

Table 1 gives the comparison of area-complexity, computation time and VLSI performance measure of the proposed bilayer structure with the structures of [12], [13] and [14].

Table 1.

Structure	Area complexity(A)	Computation time (τ)	VLSI performance measure ($A\tau^2$)
Proposed structure	N^2	$2N$	$4N^4$
[12]	N^2	$2N$	$4N^4$
[13]	$3N^2$	$2N$	$12N^4$
[14]	$(N^4-1)/2$	$(N^2+1)/2$	$(N^8+2N^6-2N^2-1)/8$

4. Proposed algorithm-2 for 2-D DST:

Using (3), (5) can be written as

$$W_{mj} = \sum_{i=1}^{N} x_{ij} \sin\left[\frac{(2i-1)m\pi}{2N}\right]$$

$$= \sum_{i=1}^{N/2}\left[x_{ij} + (-)^{m+1} x_{(N+1-i)j}\right]\sin\left[\frac{(2i-1)m\pi}{2N}\right]$$

$$= \sum_{i=1}^{N/2}\left[x_{ij} + (-)^{m+1} x_{(N+1-i)j}\right]S_{mi} \qquad (10)$$

From (3) and (4), we have

$$Y_{mn} = \sum_{j=1}^{N} W_{mj} \sin\left[\frac{(2j-1)n\pi}{2N}\right]$$

$$= \sum_{j=1}^{N/2}\left[W_{mj} + (-1)^{n+1} W_{m(N+1-j)}\right]\sin\left[\frac{(2j-1)n\pi}{2N}\right] \qquad (11)$$

$$= \sum_{j=1}^{N/2}\left[W_{mj} + (-1)^{n+1} W_{m(N+1-j)}\right]S_{nj}$$

$$= \sum_{j=1}^{N/2} Q_{mj}^{r} S_{nj} \qquad (12)$$

where

$$Q_{mj}^{r} = \left[W_{mj} + (-1)^{n+1} W_{m(N+1-j)}\right] \qquad (13)$$

with $r = 0$ for even n and $r = 1$ for odd n

5. Systolic architecture for implementation of 2-D DST using algorithm-2 for N = 4

The 2-D DST given in algorithm-2 can be realized by the following 3 steps.

1. Compute W_{mj} using (10)
2. Compute Q^r_{mj} using (13)
3. Compute Y_{mn} using (12)

The above 3 steps are implemented by systolic architectures for $N = 4$

***Step1*:**

Equation (10) for $N = 4$ can be written as

$$W_{mj} = \sum_{i=1}^{2} \left[x_{ij} + (-1)^{m+1} x_{(5-i)j} \right] S_{mi} \qquad (14)$$

for $j = 1, 2, 3, 4$ and $m = 1, 2, 3, 4$.

From (14), the following 16 expressions can be obtained for all values of j and m.

$$W_{11} = (x_{11} + x_{41})S_{11} + (x_{21} + x_{31})S_{12}$$
$$W_{21} = (x_{11} - x_{41})S_{21} + (x_{21} - x_{31})S_{22}$$
$$W_{31} = (x_{11} + x_{41})S_{31} + (x_{21} + x_{31})S_{32}$$
$$W_{41} = (x_{11} - x_{41})S_{41} + (x_{21} - x_{31})S_{42}$$
$$W_{12} = (x_{12} + x_{42})S_{11} + (x_{22} + x_{32})S_{12}$$
$$W_{22} = (x_{12} - x_{42})S_{21} + (x_{22} - x_{32})S_{22}$$
$$W_{32} = (x_{12} + x_{42})S_{31} + (x_{22} + x_{32})S_{32}$$
$$W_{42} = (x_{12} - x_{42})S_{41} + (x_{22} - x_{32})S_{42} \qquad (15)$$
$$W_{13} = (x_{13} + x_{43})S_{11} + (x_{23} + x_{33})S_{12}$$
$$W_{23} = (x_{13} - x_{43})S_{21} + (x_{23} - x_{33})S_{22}$$
$$W_{33} = (x_{13} + x_{43})S_{31} + (x_{23} + x_{33})S_{32}$$
$$W_{43} = (x_{13} - x_{43})S_{41} + (x_{23} - x_{33})S_{42}$$
$$W_{14} = (x_{14} + x_{44})S_{11} + (x_{24} + x_{34})S_{12}$$
$$W_{24} = (x_{14} - x_{44})S_{21} + (x_{24} - x_{34})S_{22}$$
$$W_{34} = (x_{14} + x_{44})S_{31} + (x_{24} + x_{34})S_{32}$$
$$W_{44} = (x_{14} - x_{44})S_{41} + (x_{24} - x_{34})S_{42}$$

The first step of 2-D DST algorithm-2 is implemented by the systolic architecture shown in Fig. 5. This architecture consists of $N/2$ adder / subtractor cells ($N = 4$ here) and $N^2/2$ PEs for calculating W_{mj} based on (10). The function of each adder /subtractor cell is shown in Fig. 6 and the function of each PE is shown in Fig. 7. Each PE consists of one multiplier, one adder and one register for storing S_{mi}. The pair of input data x_{ij} and $x_{(N+1-i)j}$ enters the adder / subtractor cell one cycle ahead of the pair $x_{(i+1)j}$ and $x_{(N-i)j}$. When the input data move-down the architecture, W_{mj} given by (15) will be generated in a manner shown in Fig. 5

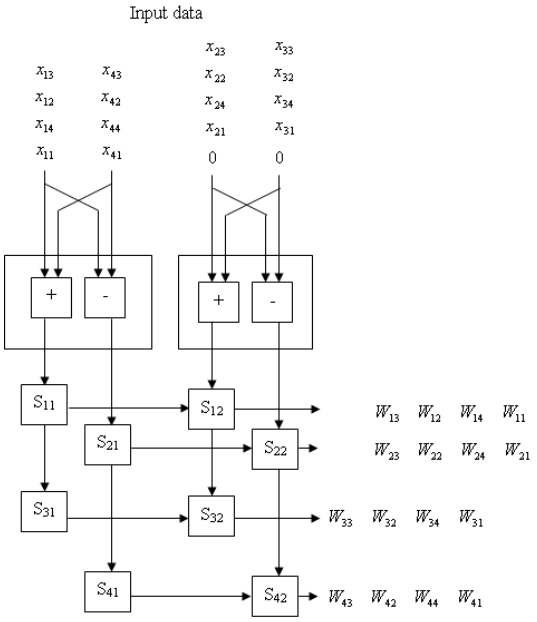


Figure 5. Systolic architecture for step-1 of 2D DST algorithm – 2 for $N = 4$.

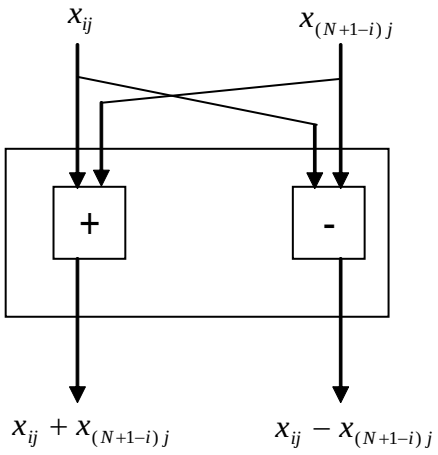
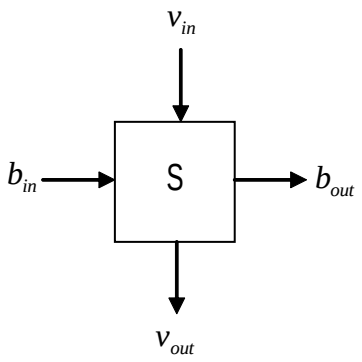


Figure 6. Adder / subtractor cell of systolic architecture for step-1 of 2D DST algorithm-2



$$b_{out} = b_{in} + Sv_{in}\ ;\ v_{out} = v_{in}$$

Figure 7. Function of each PE of systolic architecture for step–1 of 2D DST algorithm-2

***Step* 2:**

For $N = 4$, we have from (12) and (13)

$$Y_{mn} = \sum_{j=1}^{2} Q_{mj}^{r} S_{nj} \tag{16}$$

$$= \sum_{j=1}^{2} \left[W_{mj} + (-1)^{n+1} W_{m(5-j)} \right] \tag{17}$$

for $m, n = 1,2,3,4$ with $r = 0$ for even n and $r = 1$ for odd n.

From (16) and (17), we get the following 16 expressions for all values of m and n.

$$\begin{aligned}
Y_{11} &= Q_{11}^{1}\ S_{11} + Q_{12}^{1}\ S_{12} = (W_{11} + W_{14})\ S_{11} + (W_{12} + W_{13})\ S_{12} \\
Y_{21} &= Q_{21}^{1}\ S_{11} + Q_{22}^{1}\ S_{12} = (W_{21} + W_{24})\ S_{11} + (W_{22} + W_{23})\ S_{12} \\
Y_{31} &= Q_{31}^{1}\ S_{11} + Q_{32}^{1}\ S_{12} = (W_{31} + W_{34})\ S_{11} + (W_{32} + W_{33})\ S_{12} \\
Y_{41} &= Q_{41}^{1}\ S_{11} + Q_{42}^{1}\ S_{12} = (W_{41} + W_{44})\ S_{11} + (W_{42} + W_{43})\ S_{12} \\
Y_{12} &= Q_{11}^{0}\ S_{21} + Q_{12}^{0}\ S_{22} = (W_{11} - W_{14})\ S_{21} + (W_{12} - W_{13})\ S_{22} \\
Y_{22} &= Q_{21}^{0}\ S_{21} + Q_{22}^{0}\ S_{22} = (W_{21} - W_{24})\ S_{21} + (W_{22} - W_{23})\ S_{22} \\
Y_{32} &= Q_{31}^{0}\ S_{21} + Q_{32}^{0}\ S_{22} = (W_{31} - W_{34})\ S_{21} + (W_{32} - W_{33})\ S_{22} \\
Y_{42} &= Q_{41}^{0}\ S_{21} + Q_{42}^{0}\ S_{22} = (W_{41} - W_{44})\ S_{21} + (W_{42} - W_{43})\ S_{22}
\end{aligned} \tag{18}$$

$$Y_{13} = Q_{11}^{1}\ S_{31} + Q_{12}^{1}\ S_{32} = (W_{11} + W_{14})\ S_{31} + (W_{12} + W_{13})\ S_{32}$$

$$Y_{23} = Q_{21}^{1}\ S_{31} + Q_{22}^{1}\ S_{32} = (W_{21} + W_{24})\ S_{31} + (W_{22} + W_{23})\ S_{32}$$
$$Y_{33} = Q_{31}^{1}\ S_{31} + Q_{32}^{1}\ S_{32} = (W_{31} + W_{34})\ S_{31} + (W_{32} + W_{33})\ S_{32}$$
$$Y_{43} = Q_{41}^{1}\ S_{31} + Q_{42}^{1}\ S_{32} = (W_{41} + W_{44})\ S_{31} + (W_{42} + W_{43})\ S_{32}$$
$$Y_{14} = Q_{11}^{0}\ S_{41} + Q_{12}^{0}\ S_{42} = (W_{11} - W_{14})\ S_{41} + (W_{12} - W_{13})\ S_{42}$$
$$Y_{24} = Q_{21}^{0}\ S_{41} + Q_{22}^{0}\ S_{42} = (W_{21} - W_{24})\ S_{41} + (W_{22} - W_{23})\ S_{42}$$
$$Y_{34} = Q_{31}^{0}\ S_{41} + Q_{32}^{0}\ S_{42} = (W_{31} - W_{34})\ S_{41} + (W_{32} - W_{33})\ S_{42}$$
$$Y_{44} = Q_{41}^{0}\ S_{41} + Q_{42}^{0}\ S_{42} = (W_{41} - W_{44})\ S_{41} + (W_{42} - W_{43})\ S_{42}$$

Figure 8 shows a circuit for systolic implementation of step-2 of 2-D DST algorithm-2. It consists of N cells (N = 4 here) to realize Q_{mj}^{r} given in (13). The inputs of this circuit are the output data of the systolic architecture shown in Fig. 5. Each cell is connected to a control signal C of sequence 0101…., which is synchronized to the input data sequence. Each cell performs one addition and one subtraction alternately for the same input data. Delay elements Z^{-1} are connected to the cells for arranging the data flow Q_{mj}^{r}. The output of the cell is Q_{mj}^{1} if C = 1 and Q_{mj}^{0} if C = 0.

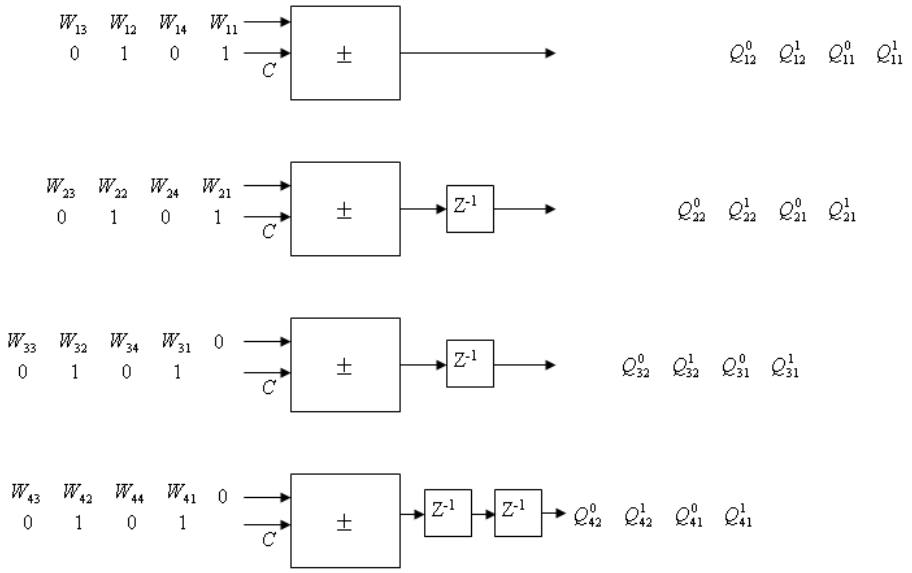


Figure 8. Circuit for systolic implementation of step-2 of 2D DST algorithm-2 for N = 4

***Step* 3:**

To realize the final step-3 of 2-D DST algorithm-2, the systolic architecture shown in Fig.9 is used. This architecture contains $N^2/2$ PEs and some delay elements Z^{-1} to compute Y_{mn} based on (12). The output data of the circuit in Fig. 8 enters this array from left, where as the stream of S_{nj} move down the architecture. The function of each PE is shown in Fig.10. Each PE contains two accumulators A_1 and A_2. Each PE is connected to a control signal C of sequence 0101……. When C = 0, the content of A_1 is used and when C = 1, the content of A_2 is used. The output Y_{mn} given in (18) is realized by this architecture.

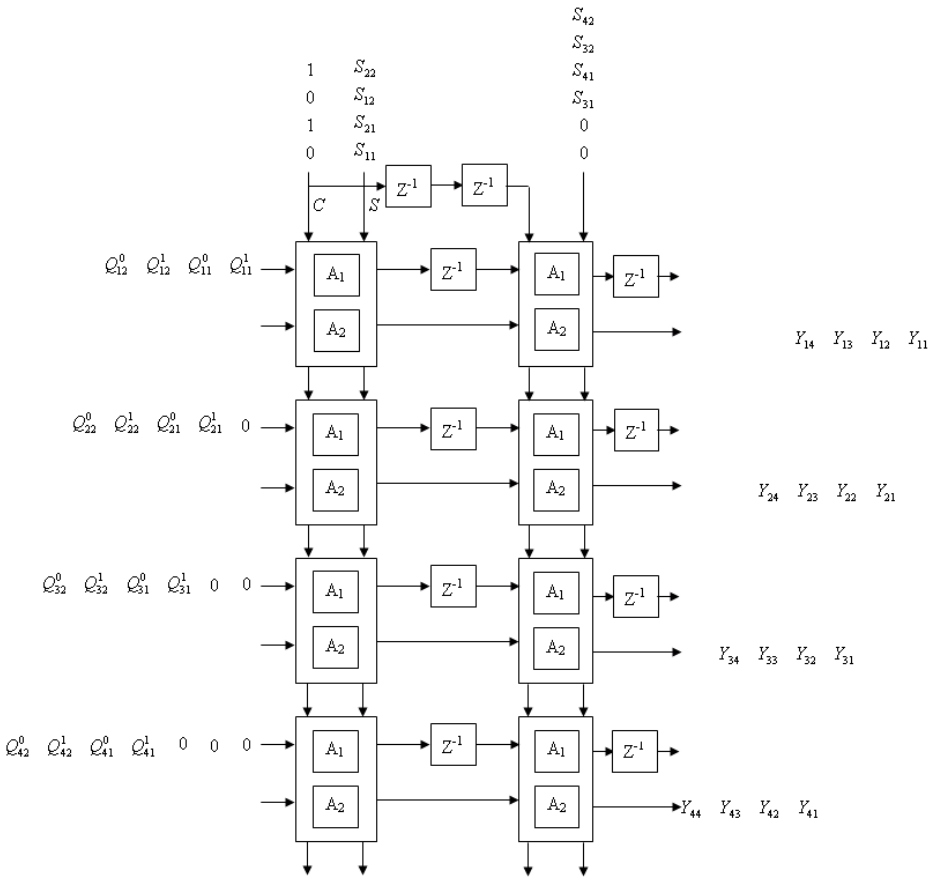


Figure 9. Systolic architecture for step – 3 of 2-D DST algorithm-2 for $N = 4$

$S' = S$ $\quad A_1 \leftarrow A_1 + Sv_i$ for $C = 0$

$C' = C$ $\quad A_2 \leftarrow A_2 + Sv_i$ for $C = 1$

$v_0 = v_i$ $\quad y' \leftarrow A_1$ then $y' \leftarrow A_2$

$y' = y$

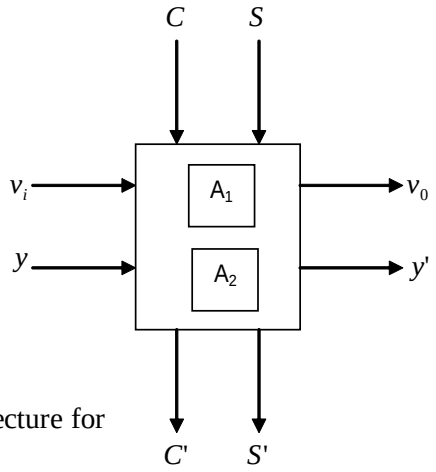


Figure 10. Function of each PE of systolic architecture for step-3 of 2D DST algorithm-2.

The complete systolic architecture for implementation of 2-D DST algorithm-2 can be obtained by combining the arrays shown in Fig. 5, Fig. 8. and Fig. 9. This complete systolic architecture requires N^2 multipliers and $N^2 + 3N$ adders.

6. Conclusion

In this paper, two algorithms for realizing two-dimensional discrete sine transform (2-D DST) are proposed. Basing on these two algorithms, two systolic architectures are presented for implementing 2-D DST of even length N.

The systolic array using the algorithm-1 is a bilayer structure, which does not require any hardware/time for the transposition of the intermediate results. It provides high throughput of computation due to fully pipelined processing and massive parallelism. It is observed that the proposed bilayer structure involves significantly less area-complexity, less computation time and provides better VLSI performance measure compared with other two structures [13] and [14]. The bilayer structure permits data to be moved both horizontally and vertically. This helps to boost the performance of the structure.

The systolic architecture basing on algorithm-2 consists of four different types of basic cells and possesses regularity, modularity and local connections. Therefore, this architecture is suitable for VLSI implementation. This systolic architecture requires N^2 multipliers and $N^2 + 3N$ adders.

The systolic arrays are used in the design and implementation of high performance digital signal processing equipment. The systolic array concept can also be exploited at bit level in the design of individual VLSI chips. The highly regular structure of systolic circuits renders them comparatively easy to design and test.

7. References

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