



ISSN 2231-3478

(Print)

JUSPS-B Vol. 29(10), 285-291 (2017). Periodicity-Monthly

Section B

(Online)



ISSN 2319-8052

9 772319 805003



Estd. 1989

JOURNAL OF ULTRA SCIENTIST OF PHYSICAL SCIENCES
An International Open Free Access Peer Reviewed Research Journal of Physical Sciences
website:- www.ultrascientist.org

Simulation of Co-axial Carbon Nanotube Field Effect Transistor (CNTFET) using Nanohub

¹G.K. PANDEY, ²U.N. TRIPATHI and ³MANISH MISHRA

^{1,3}Department of Electronics, D.D.U. Gorakhpur University, Gorakhpur-273009 (India)

²Department of Computer Science, D.D.U. Gorakhpur University, Gorakhpur-273009 (India)

Corresponding Author E-manish.ddu1976@gmail.com

<http://dx.doi.org/10.22147/jusps-B/291005>

Acceptance Date 5th September, 2017, Online Publication Date 2nd October, 2017

Abstract

In this paper, the design and simulation of cylindrical, co-axial, Carbon Nanotube Field Effect Transistor (CNTFET) is presented using online Fettoy tool of Nanohub. This tool can provide various characteristics of CNTFET, like transfer characteristics, output characteristics, average velocity vs. gate voltage etc. To simulate the CNTFET we have considered the value of diameter of carbon nanotube 1nm which is of (13,0) chirality. Gate insulator thickness is taken as 1.5nm and the dielectric constant of the material used as gate oxide is $k=20$, which is the value shown by ZrO_2 .

A comparison between designed CNTFET and conventional MOSFET shows improvement of various parameters which plays a significant role in design of logic circuits. With these improved properties of CNTFETs it can be concluded that it is very useful in designing of reversible logic circuits. Also, it is very efficient in terms of power consumption, speed of operations, and leakage current over conventional MOSFETs.

Key words : Carbon Nanotube, Field effect transistor, Simulation, FETToy.

I. Introduction

In the Carbon nanotube Field Effect Transistor (CNTFET) technology the single wall carbon nanotube (SWCNT) is generally used as a channel between source and drain in CNTFET¹. Both p-channel and n-channel devices can be made from nanotubes. The physical structure of CNTFETs is very similar to that of MOSFETs and their I-V characteristics and transfer characteristics are also very promising and they suggest that CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics. The carbon nanotube has following properties that make it useful in making of CNTFETs².

1. SWCNT can be semiconducting or metallic and semiconducting depending upon the chiral vector.
2. The energy gap of semiconducting carbon nanotubes can be varied continuously by varying the nanotube diameter. Here the band gap of semiconducting nanotubes decreases with increasing diameter³.
3. In SWCNT the transport of charge carriers (i.e. electrons/holes) is one dimensional and backscattering is strongly suppressed resulting in high mobility of charge carriers due to which the on-current of FET become high⁴.
4. Since there are confinement of charge carriers inside the nanotube due to which nanotube allows better control of electrostatics.
5. In nanotube electron and hole transportation is equal therefore there is no any difference between the characteristic of n-type or p-type CNTFET⁵.
6. The nanotube conducts essentially on its surface where all the chemical bonds are saturated and stable. In other words, there are no dangling bonds which form interface states. Therefore, there is no need for careful passivation of the interface between the nanotube channel and the gate dielectric, i.e. there is no equivalent of the silicon/silicon dioxide interface⁶.
7. The Schottkey barrier at the metal-nanotube contact is the active switching element in an intrinsic nanotube device⁷.

II. Co-axial (Cylindrical) CNTFETs :

In co-axial CNTFET the carbon nanotube channel is surrounded by oxide layer which is further surrounded by metallic cylindrical gate contact on which the gate voltage is applied. Figure 1 shows the schematic diagram of cylindrical CNTFET⁸.

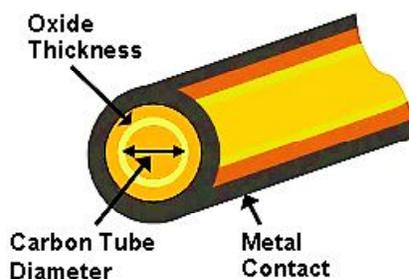


Figure 1: Cylindrical or Co-axial CNTFET

To simulate the cylindrical CNTFET the online Fettoy tool of NanoHub developed by Anisur Rahman, Purdue University is applied in this problem. This tool can provide various characteristic for CNTFETs like Transfer characteristic, Output characteristic, Average velocity vs. Gate voltage etc.

For the simulation of this CNTFET, the value of diameter of carbon nanotube is taken to be 1 nm which is of (13,0) chirality, gate insulator thickness of this CNTFET is taken 1.5 nm and the dielectric constant of the material used as gate oxide is ($K = 20$) which is for ZrO_2 .

The transfer characteristic (I_d vs. V_{gs}) of the co-axial CNTFET is shown in the figure 2. From the transfer characteristics, the value of I_{on} and I_{off} current is obtained. It is clear that the characteristics of co-axial CNTFETs are also similar to the characteristics of conventional MOSFETs. It can be inferred that the transfer characteristics of co-axial CNTFET shows improved performance in terms of threshold voltage and the on-current to off-current ratio.

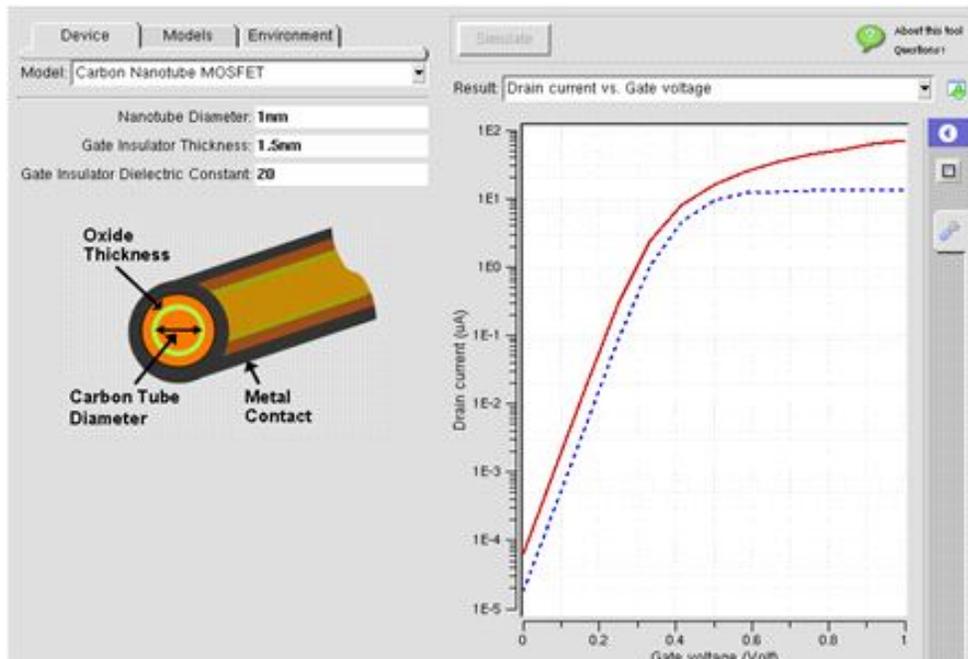


Figure 2 The $I_d \sim V_g$ characteristics of CNTFET on the Interface of Fettoy tool

Figure 3 shows the output ($I_D \sim V_D$) characteristics of the co-axial CNTFETs which is similar to the conventional MOSFET. From the curve, it is clear that the drain current remains zero as long as the gate voltage is below threshold voltage and it increases as the Gate voltage increases. Linear region and saturation region is apparent in the curve.

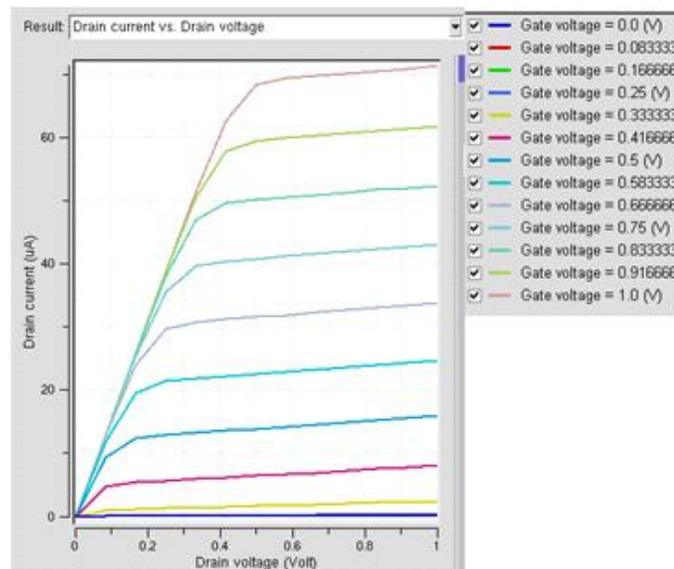


Figure 3: Output characteristics of co-axial CNTFET at different Gate voltage.

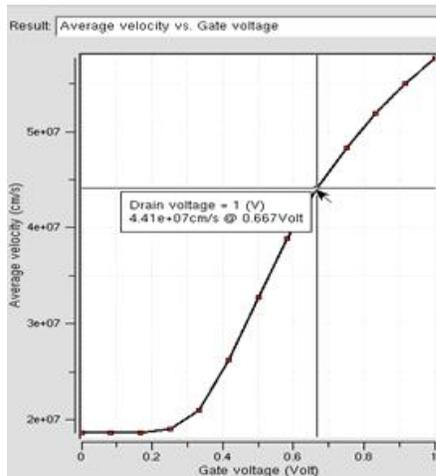


Figure 4: Average velocity vs. Gate voltage curve

Figure 4 shows the curve plotted between average velocity of charge carriers and the gate voltage. From this curve, it is clear that as the gate voltage increases at fixed drain voltage, the average velocity of charge carrier at the start, remains constant; but after certain gate voltage the velocity of charge carriers increases linearly. Other characteristics of interest which is obtained from the numerical Fettoy simulator tool are given in figure 5 and 6.

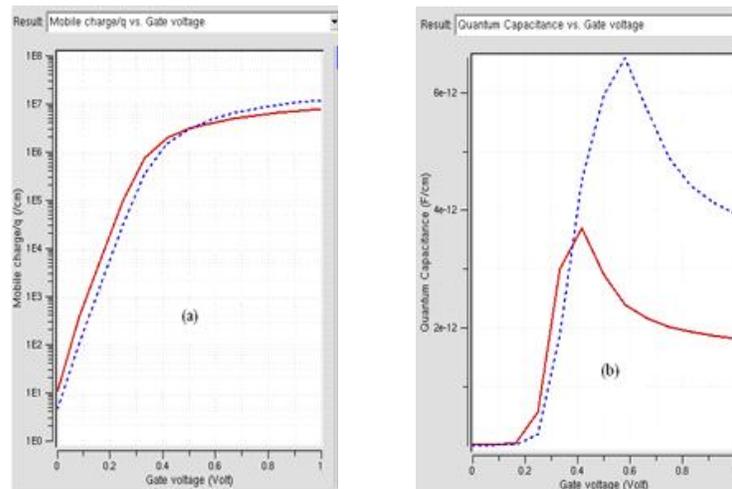


Figure 5: (a) Shows the Mobile charge Vs. Gate voltage characteristics
(b) Shows the Quantum capacitance vs. Gate voltage characteristics

Figure 5(a) shows the variation between concentration of mobile charge with the gate voltage at constant drain voltage. From this curve it can be inferred that initially the concentration of mobile charge increases linearly but beyond certain gate voltage, the mobile charge concentration get saturated which finally results to the saturation of current. Figure 5(b) shows variation between Quantum capacitance with Gate voltage. Figure 6 shows the characteristics of mobile charge concentration with the Drain voltage at constant Gate voltage.

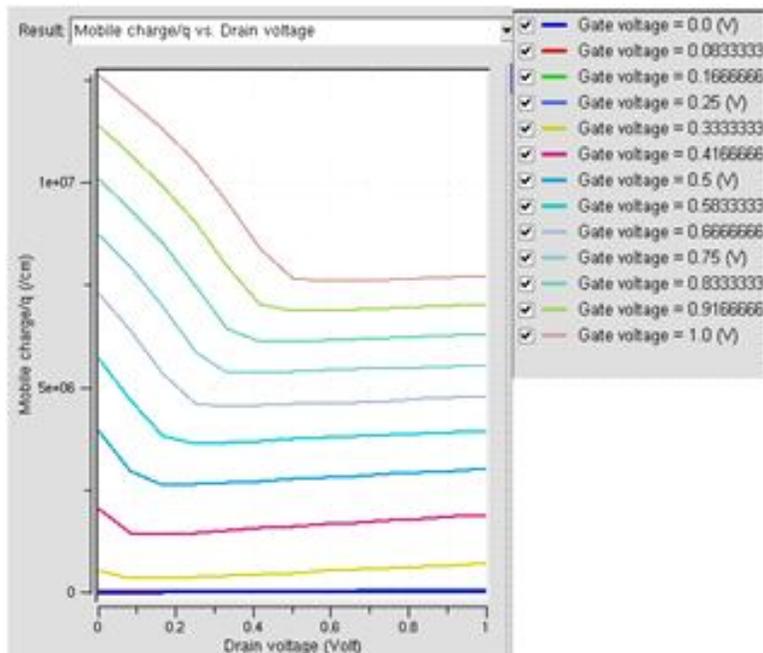


Figure 6: Concentration of mobile charge vs. Drain voltage at constant Gate voltage

III. Simulation Parameters

Following are the input simulation parameter provided to Fettoy simulator:

Gate insulator thickness	: 1.5×10^{-9} (m)
Insulator dielectric constant	: 20
Temperature	: 300 ($^{\circ}$ K)
Initial gate voltage	: 0 (eV)
Final gate voltage	: 1 (V)
Number of bias points (gate)	: 13
Initial drain voltage	: 0 (eV)
Final drain voltage	: 1 (V)
Number of bias points (drain)	: 13
Threshold voltage	: 0.32(V)
Series Resistance	: 0Ω
Nanotube diameter	: 10^{-9} (m)
Gate control parameter	: 0.88
Drain control parameter	: 0.035

IV. Result

The simulation of co-axial CNTFETs is demonstrated in figure 7, where the output characteristics and transfer characteristic are shown with the variation in diameter of carbon nanotube.

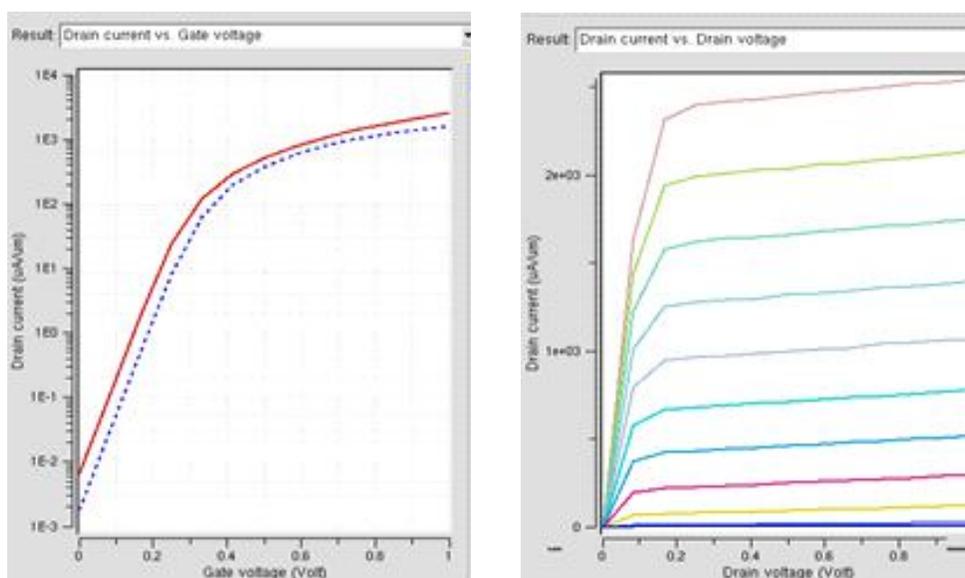


Figure 7: (a) Gate voltage (V_G) ~ Drain current (I_D), (b) Drain voltage (V_D) ~ Drain current (I_D) plots for cylindrical CNTFET

Transfer characteristics for different diameters of CNT are plotted in figure 7(a), which shows that the effect of diameter is more significant in lower region of gate bias. The switching speed is more for larger diameter i.e. as the diameter increases the device approaches to saturation faster. Figure 7(b) shows the output characteristics for different diameters of CNT used in the channel region. From the figure, it is clear that the drain current is more for higher values of diameter.

V. Conclusion

From the characteristic of co-axial CNTFETs it can be observed that the I_{on} for this structure is $71.3 \mu A$ and the I_{off} (off-current) is found $0.6 pA$ at the drain voltage of 1 volt. Hence, the ratio I_{on}/I_{off} of CNTFET is greater than conventional MOSFET which allows very less leakage current compared to the conventional MOSFET of same node technology. The CNTFETs can be operated with supply voltage ranging from 0.5V-0.7V, whereas, this range is 1.1 to 1.3 V for conventional MOSFET. In case of Si-MOSFET switching occurs by altering the channel resistivity but for CNTFET switching occurs by the modulation of contact resistance. CNTFETs are capable of delivering three to four times higher drive current than the Si-MOSFET at an overdrive of 1 volt. The on-current performance advantage of the CNTFET is either due to the high gate capacitance or due to the improved channel transport. The improved channel velocity for the CNTFET is due to the increased mobility and band structure of CNTFET. CNTFET has about four times higher transconductance compared to MOSFETs. The average carrier velocity in CNTFET is almost double that in MOSFET. The CNTFETs can be used as ambipolar devices so that a single CNTFET can be behaved as both n-type and p-type CNTFET, which is impossible with the conventional Si-MOSFETs.

With these properties of CNTFETs it can be concluded that it is very useful in designing of Logic circuits. It is very efficient in terms of power consumption, speed of operations, leakage current and many other demerits of conventional MOSFETs are either removed or reduced significantly.

VI. References

1. Michael Loong Peng Tan., G. Lentaris, G. Amartunga “Device and circuit-level performance of carbon nanotube field-effect transistor with benchmarking against a nano-MOSFET”, *Nanoscale Res Lett.*; *7(1)*, 467 (2012).
2. Shirazi SG, Mirzakuchaki S “Study of carbon nanotube field effect transistors performance based on changes in gate parameters” *J Nanosci Nanotechnol*, Dec; *11(12)*, 10424-8 (2011).
3. Toshinori Numata “Control of Threshold-Voltage and short-Channel Effect in Ultrathin Strained-SOI CMOS Devices”. *IEEE Transactions on Electron Devices*, Vol. 52, No. 8, August, 1780-1786 (2005).
4. C. Ahn, S. W. Fong, Y. Kim, S. Lee A. Sood, C. M. Neumann, M. Asheghi, K.E. Goodson, E. Pop, H.-S. P. Wong, “Energy-Efficient Phase-Change Memory with Graphene as a Thermal Barrier,” *Nano Letters*, *15 (10)*, pp 6809–6814 (2015).
5. Riichiro Saito, “Physical Properties of Carbon Nanotubes”. London. Imperial College Press (1998).
6. Peter J.F. Harris “Carbon Nanotubes and Related Structure”, Cambridge University Press, (2001).
7. S. J. Wind *et al.*, “Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes”, *Applied Physics Letters*, May, 3817-3819 (2002).
8. R. Martel, T. Schmidt, H.R. Shea, T. Hertel, and Ph. Avouris, “Single- and Multi-wall Carbon Nanotube Field-effect Transistors”, *Applied Physics Letters*, October, 2447 (1998).
9. H.-S. P. Wong and S. Salahuddin, “Memory Leads the Way to Better Computing,” *Nature Nanotechnology*, Vol. *10*, pp. 191 – 194 (2015).
10. Z. Jiang, Y. Wu, S. Yu, L. Yang, K. Song, Z. Karim, H.-S. P. Wong, “A Compact Model for Metal–Oxide Resistive Random Access Memory With Experiment Verification,” *IEEE Trans. Electron Devices*, vol. *63*, No. 5, pp. 1884 – 1892 (2016).
11. S. Lee, A. Tang, S. Aloni, H.-S. P. Wong, “Statistical Study on the Schottky Barrier Reduction of Tunneling Contacts to CVD Synthesized MoS₂,” *Nano Lett.*, *16 (1)*, pp 276–281 (2016).
12. M.M. Sabry Aly, M. Gao, G. Hills, C.-S. Lee, G. Pitner, M.M. Shulaker, T.F. Wu, M. Asheghi, J. Bokor, F. Franchetti, K.E. Goodson, C. Kozyrakis, I. Markov, K. Olukotun, L. Pileggi, E. Pop, J. Rabaey, C. Re, H.-S. P. Wong, S. Mitra, “Energy-Efficient Abundant-Data Computing: The N3XT 1,000X,” *IEEE Computer*, pp. 24–33, December (2015).
13. C.S. Lee, E. Pop, A. Franklin, W. Haensch, H.-S. P. Wong, “A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-nm Regime—Part II: Extrinsic Elements, Performance Assessment, and Design Optimization,” *IEEE Trans. Electron Devices*, vol. *62*, no. 9, pp. 3070-3078 (2015).
14. M. M. Shulaker, G. Hills, M. Giachino, T.F. Wu, Z. Bao, H.-S. P. Wong, and S. Mitra, “Efficient Metallic Carbon Nanotube Removal for Highly-Scaled Technologies,” *IEEE International Electron Devices Meeting (IEDM)*, paper 32.4, pp. 839 – 842, Washington, DC, December 7 – 9, (2015).