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# Design and Simulation of Reconfigurable Logic Circuits using CNTFETs

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## Abstract

In the proposed paper the basic logical cells like inverter, NOR and NAND are realized using n-type and p-type CNTFET. These blocks are used to implement seven function reconfigurable logic blocks. The VHDL code, simulation and synthesized results are generated on Xilinx 9.2 platform. The designed circuit is FPGA programmed on Altera kit.

**Keywords :** CNTFET, Reconfigurable logic, Xilinx, FPGA, MOSFET.

## I. Introduction

As with the conventional MOSFET, there also exist two types of CNTFETs, *i.e.* n-channel and p-channel CNTFETs<sup>1</sup>, the circuit symbol of which is shown in figure 1.

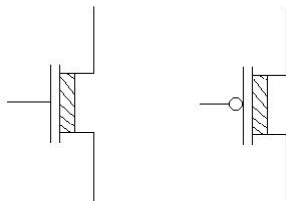


Figure 1: Circuit Symbol of n-channel and p-channel CNTFET.

With the help of these CNTFETs, the logic gates like inverter, NAND and NOR can be realized<sup>2</sup>. The circuit of these gates using CNTFET is shown in figure 2.

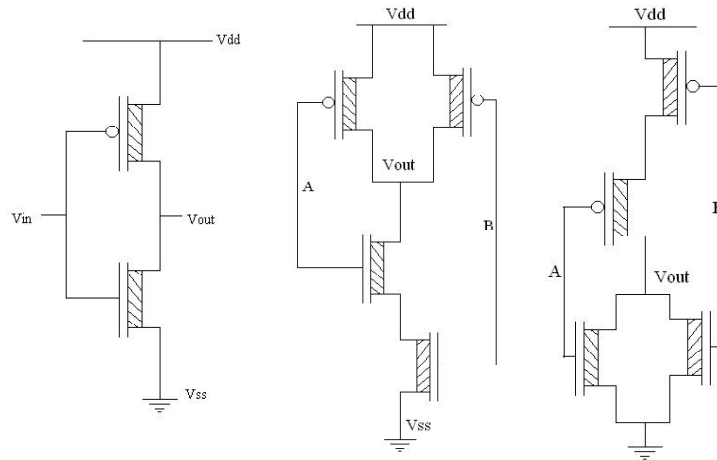


Figure 2: CNTFET Logic Circuits (a) Inverter, (b) two input NAND, (c) two input NOR

The voltage transfer characteristics of the CNT-FET inverter are similar to the voltage transfer characteristics of a typical CMOS inverter and show a sharp transition at the inverter logic threshold voltage<sup>3</sup>. With the help of these logic building blocks we proceed to design the reconfigurable circuit of seven functions, the block diagram of which is shown in figure 3. The block contains two input pins, three mode selection pin and one output pin. On the input pins desired binary input is provided and on the select pins binary pattern is applied to select one out of seven modes of operation as AND, OR, NOT, NAND, NOR, XOR and XNOR gate. The VHDL code of this entity is generated and synthesized on Xilinx platform.

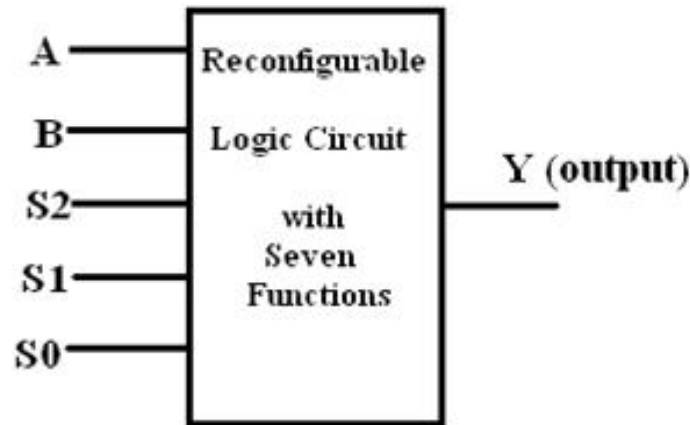


Figure 3: Reconfigurable Logic Block

The function of select input pin is given in table I, which describes the mode of operation of circuit which is obtained by giving the proper signal on the select lines and output is obtained by applying input at **A** and **B**.

Table I: Functions of Select Pins

Select Mode			Gate Function
S2	S1	S0	
0	0	0	AND
0	0	1	OR
0	1	0	NOT
0	1	1	NAND
1	0	0	NOR
1	0	1	XOR
1	1	0	XNOR
1	1	1	X (Don't care)

## II VHDL Coding

The logic equation and VHDL coding of the proposed reconfigurable logic circuit is given below. The dataflow style of circuit modeling is adopted for this design.

$$Y = \bar{A} S1 \bar{S2} + \bar{A} \bar{B} S1 + S0 (A \oplus B) + AB (S1 \odot S2) \quad (1)$$

```

library ieee;
use ieee.std_logic_1164.all;
entity recon is
port( a,b,s2,s1,s0 : in std_logic;
y : out std_logic);
end recon;
architecture recon of recon is
signal x0,x1,x2,x3,x4,x5,x6,x7,x8,x9,x10 : std_logic;
begin
    x0 <= not(a);
    x1 <= not(b);
    x2 <= not(s2);
    x3 <= not(s0);
    x4 <= x0 and x2 and s1;
    x5 <= x0 and x1 and s1;
    x6 <= x0 and x1 and x3 and s2;
    x7 <= a xor b;
    x8 <= not(s1 xor s2);
    x9 <= x7 and s0;
    x10 <= x8 and a and b;
    y <= x4 or x5 or x6 or x9 or x10;
end recon;

```

## III Circuit Diagram

The proposed structure of the reconfigurable logic gate with the help of p-type and n-type CNTFETs on the basis of CMOS logic is given in the figure 5. In this circuit, the pull-up network is made up of p-type of CNTFETs and the pull-down network is made up of n-type CNTFETs. In the design of circuit with the help of CMOS logic, a total of 30 p-type and 30 n-type CNTFETs are needed; thus, a total of 60 CNTFETs are required to design the proposed reconfigurable block.

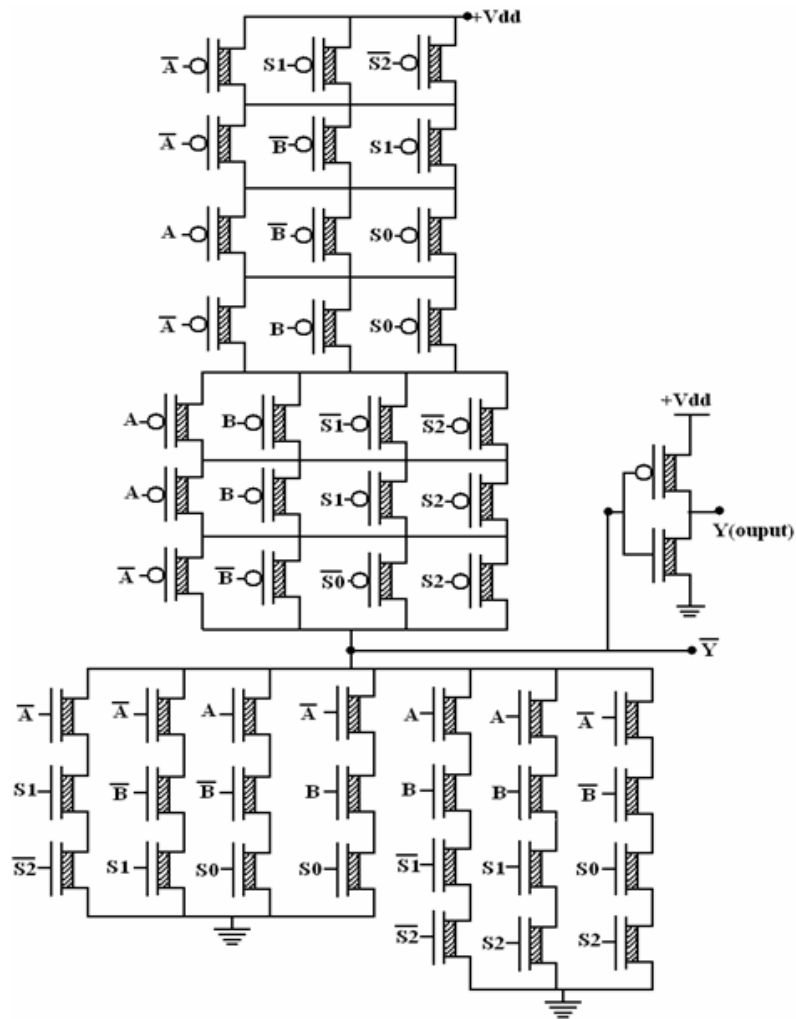


Figure 5: Design of Reconfigurable Logic made up of CNTFET

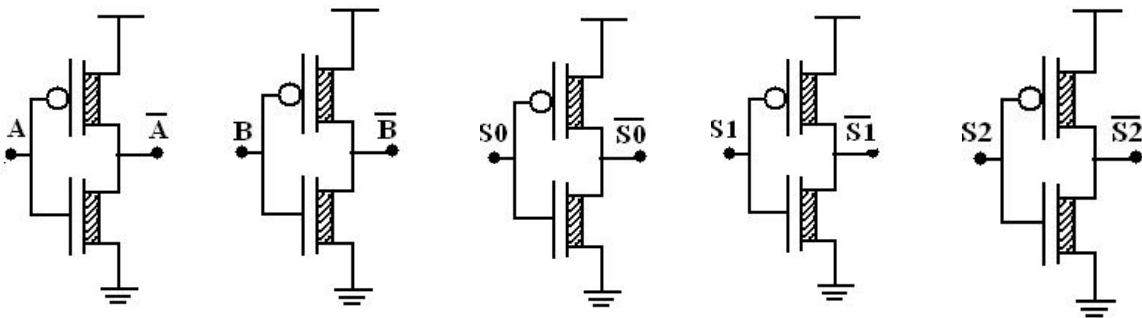


Figure 6: Generation of desired signals in figure 5 with the help of CNTFETs

#### IV Circuit Synthesis on Altera FPGA

The synthesized output waveform on Altera FPGA is shown in figure 7. From the generated output it is observed that reconfigurable circuit works as described in table I.

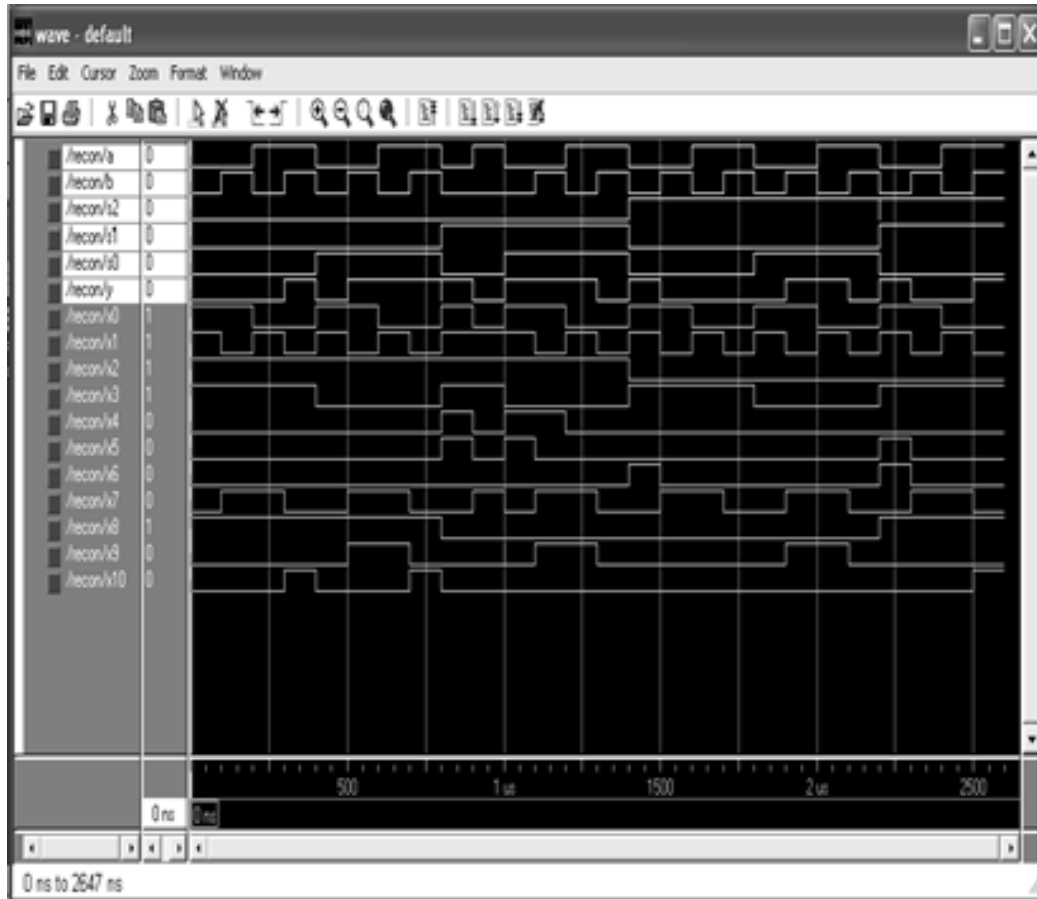


Figure 7: Synthesized Waveform

#### V. Conclusion

As a circuit component the top gate planner CNTFET and co-axial CNTFET are more efficient to design VLSI circuits at nanometer scale than the conventional Si-MOSFET, therefore, the reconfigurable logic gate circuits designed with the help of CNTFET would also be more efficient in terms of switching speed, leakage current, on-current to off-current ratio, and power dissipation.

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